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EXAMINER	
DINH, DUC Q	

ART UNIT	PAPER NUMBER
2629	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/821,847	KANEKO ET AL.	
	Examiner	Art Unit	
	DUC Q. DINH	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 April 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *4/12/04;9/7/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-7 rejected under 35 U.S.C. 102(e) as being anticipated by Mizutani et al. (U.S Patent No. 6,392,620), hereinafter Mizutani.

In reference to claim 1, Mizutani discloses a picture image display device (Fig. 1) comprising pixels which are formed in a matrix shape (Fig. 2) defined by a plurality of gate lines and a plurality of data lines crossing thereto and each including an electro optical element (liquid crystal of the display is an optical element) and a switching element (TFT 5), wherein the pixels are driven while introducing a light quenching period (i.e. F12 Fig. 3B) in which the electro optical element is caused to be quenched after the plurality of gate lines being scanned for displaying one picture image (Figs 3; col. 3,lines 50 67; col. 4, lines 1-7).

In reference to claim 2, Mizutani discloses an active matrix type picture image display device comprising pixels which are formed in a matrix shape defined by a plurality of gate lines and a plurality of data lines crossing thereto and each including an electro optical element and a switching element, wherein the pixels are driven while introducing a light quenching period, in which the electro optical elements are caused to be quenched, in one frame period for displaying one picture image. (see the rejection of Claim 1)

In reference to claim 3, Mizutani picture image display device comprising pixels which are formed in a matrix shape defined by a plurality of gate lines to which scanning signals are fed and a plurality of data lines crossing thereto to which picture image signals are fed and each including an electro optical element and a thin film transistor, wherein the pixels are driven while introducing a light quenching period, in which the electro optical element is caused to be quenched, by feeding scanning signals to the plurality of gate line as well as picture image signals to the plurality of data lines after feeding scanning signals to the plurality of gate lines for displaying one picture image. (See rejection as applied to claim 1)

In reference to claim 4, Mizutani discloses a picture image display device for displaying motion picture images comprising pixels which are formed in a matrix shape defined by a plurality of gate lines to which scanning signals are fed and a plurality of data lines crossing thereto to which picture image signals are fed and each including an electro optical element and a thin film transistor,, wherein the pixels are driven while introducing a light quenching period, in which the electro optical elements are caused to be quenched, by feeding scanning signals to the plurality of gate lines as well as feeding picture image signals for quenching the electro optical elements to the plurality of data lines in synchronism with the scanning signal after feeding the scanning signals to the plurality of gate lines and causing the electro optical element light emission for displaying one picture image, thereby a blurred edge of a motion picture image is prevented. (see the rejection of claim 1; in addition Mizutani discloses the invention is to reduce an afterimage phenomenon for displaying moving image, i.e. blurred edge of a motion picture is prevented; col. 1,lines 32-40).

In reference to claim 5, Mizutani discloses picture image display device comprising pixels which are formed in a matrix shape defined by a plurality of gate lines to which scanning signals are fed and a plurality of data lines crossing thereto to which picture image signals are fed and each including an electro optical element and a thin film transistor, wherein the pixels are driven while introducing a light quenching period, in which the electro optical elements are caused to be quenched, in one frame period for displaying one picture image, and in the light quenching period scanning signals are fed to the plurality of gate lines as well as picture image signals for quenching the electro optical elements are fed to the plurality of data lines in synchronism with the scanning signals (see rejection of claim 1; col. 4, lines 7-17).

In reference to claim 6, Mizutani discloses a picture image display device comprising pixels which are formed in a matrix shape defined by a plurality of gate lines to which scanning signals are fed and a plurality of data lines crossing thereto to which picture image signals are fed and each including an electro optical element and a thin film transistor, and further comprising a display control controller which introduces a light quenching period, in which the electro optical elements are caused to be quenched in one frame period for displaying one picture image, and feeds scanning signals to the plurality of gate lines as well as picture image signals for quenching the electro optical elements to the plurality of data lines in synchronism with the scanning signals in the light quenching period. (see rejection of claim 1; col. 4, lines 7-17).

In reference to claim 7, Mizutani discloses a picture image display device for displaying motion picture images comprising pixels which are formed in a matrix shape defined by a plurality of gate lines to which scanning signals are fed and a plurality of data lines crossing thereto to which picture image signals are fed and each including an electro optical element and a

thin film transistor, wherein the pixels are driven in such a manner that while introducing a light quenching period, in which the electro optical elements are caused to be quenched, between one frame period for displaying one picture image and another frame period for displaying subsequent one picture image, and scanning signals are fed to the plurality of gate lines as well as picture image signals for quenching the electro optical elements are fed to the plurality of data lines in synchronism with the scanning signals in the light quenching period (see rejection of claim 6).

In reference to claim 8, Mizutani discloses a picture image display device according to claim 3, wherein each pixel includes a first thin film transistor to which the scanning signals are fed via the gate line, a capacitor which holds the picture image signals fed from the data line via the first thin film transistor, a second thin film transistor to which the picture image signals held in the capacitor are fed and an electro optical element which is caused light emission by a drive current flowing between a pixel electrode and an opposing electrode of the electro optical element when the pixel electrode is electrically connected to a common potential line via the second thin film transistor. (see rejection of claim 6)

In reference to claim 9, Mizutani discloses a picture image display device according to claim 4, wherein each pixel includes a first thin film transistor to which the scanning signals are fed via the gate line, a capacitor which holds the picture image signals fed from the data line via the first thin film transistor, a second thin film transistor to which the picture image signals held in the capacitor are fed and an electro optical element which is caused light emission by a drive current flowing between a pixel electrode and an opposing electrode of the electro optical

element when the pixel electrode is electrically connected to a common potential line via the second thin film transistor. (see rejection of claim 8)

In reference to claim 10, Mizutani discloses wherein each pixel includes a first thin film transistor (5 of Fig. 2) to which the scanning signals are fed via the gate line, a capacitor (7 of Fig. 2) which holds the picture image signals fed from the data line via the first thin film transistor, a second thin film transistor (6) to which the picture image signals held in the capacitor are fed and an electro optical element which is caused light emission by a drive current flowing between a pixel electrode (1b) and an opposing electrode (1a of Fig. 2) of the electro optical element when the pixel electrode is electrically connected to a common potential line via the second thin film transistor (6 of Fig. 2) [see Fig. 2].

In reference to claim 11, Mizutani disclsoes a picture image display device according to claim 6, wherein each pixel includes a first thin film transistor to which the scanning signals are fed via the gate line, a capacitor which holds the picture image signals fed from the data line via the first thin film transistor, a second thin film transistor to which the picture image signals held in the capacitor are fed and an electro optical element which is caused light emission by a drive current flowing between a pixel electrode and an opposing electrode of the electro optical element when the pixel electrode is electrically connected to a common potential line via the second thin film transistor. (see rejection of claim 10)

In reference to claim 12, Mizutani discloses a picture image display device according to claim 7, wherein each pixel includes a first thin film transistor to which the scanning signals are fed via the gate line, a capacitor which holds the picture image signals fed from the data line via the first thin film transistor, a second thin film transistor to which the picture image signals held

in the capacitor are fed and an electro optical element which is caused light emission by a drive current flowing between a pixel electrode and an opposing electrode of the electro optical element when the pixel electrode is electrically connected to a common potential line via the second thin film transistor. (see rejection of claim 10)

In reference to claim 13, Mizutani discloses wherein the gate lines, the data lines, the first thin film transistors, the second thin film transistors, the capacitors and the electro optical elements are mounted on a common substrate (substrate 3b in Fig. 1; col. 3, lines 5-13).

In reference to claim 14, Mizutani discloses wherein the gate lines, the data lines, the first thin film transistors, the second thin film transistors, the capacitors and the electro optical elements are mounted on a common substrate. (substrate 3b in Fig. 1; col. 3, lines 5-13)

In reference to claim 15, Mizutani discloses wherein the gate lines, the data lines, the first thin film transistors, the second thin film transistors, the capacitors and the electro optical elements are mounted on a common substrate. 16. A picture image display device according to claim 11, wherein the gate lines, the data lines, the first thin film transistors, the second thin film transistors, the capacitors and the electro optical elements are mounted on a common substrate (substrate 3b in Fig. 1; col. 3, lines 5-13).

In reference to claim 17, Mizutani discloses wherein the gate lines, the data lines, the first thin film transistors, the second thin film transistors, the capacitors and the electro optical elements are mounted on a common substrate. (substrate 3b in Fig. 1; col. 3, lines 5-13)

Response to Arguments

3. Applicant's arguments regarding the Restriction/Election Requirement with respect to claim 1-17 have been considered and persuasive. The Restriction/Requirement hereby withdrawn.

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to DUC Q. DINH whose telephone number is (571) 272-7686. The examiner can normally be reached on Mon-Fri from 8:00.AM-4:00.PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, RICHARD HJERPE can be reached on (571)272-7691. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DUC Q DINH
Examiner
Art Unit 2629